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Review Article

An Effective Modulation Technique for Multi Level Inverters

Essam Hendawi[1*]

[1]Department of Electrical Engineering, College of Engineering, Taif University, P. O. Box 11099, Taif 21944, Saudi Arabia

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***Corresponding author:** Essam Hendawi
Department of Electrical Engineering, College of Engineering, Taif University, P. O. Box 11099, Taif 21944, Saudi Arabia

Abstract

High frequency modulation techniques play very important role in multilevel inverters MLIs. These techniques have several advantages over low frequency modulation methods where they provide lower harmonic contents and higher performance in real time adaptation. Multicarrier sinusoidal pulse width modulation MCSPWM is a common high frequency technique and control method for MLIs. The synchronization of carrier signals, complexity of hardware components and high cost are very important issues when implementing multicarrier MCSPWM in real time. This paper presents an efficient approach that can overcome the problems of multicarrier signals. The proposed approach combines the advantages of low and high frequency modulation techniques. Real time adaptation of modulation index can be achieved easily, and harmonics contents are reduced to very low levels as well. Simulation and comparison of the proposed approach with MCSPWM are presented. The proposed approach is applied and tested effectively with different topologies of MLIs.

Keywords: Multicarrier signals; sine-wave signal; Higher level modulation; MLI; total harmonic distortion.

1. INTRODUCTION

Multilevel inverters (MLIs) have become very popular due to their several advantages over conventional two-level DC-AC inverters. MLIs possess very low total harmonic distortion (THD), low voltage stresses across power electronic switches, and low electromagnetic interference (EMI). MLIs have been globally recognized in enormous applications such as renewable energy systems, electric vehicles, AC motor drives, uninterrupted power supplies and flexible AC transmission [1-4]. Several topologies of MLIs are presented in the literature including single phase and three phase MLIs. According to MLI power circuit, MLIs can be classified into three popular types; neutral point clamped (NPC) inverters, cascaded H-bridge (CHB) inverters and flying capacitors (FC) inverters [5-8]. Each topology has its own advantages and disadvantages regarding the number of possible levels, level to switch ratio (LSR), total harmonic distortion (THD), modularity, etc [9-12]. Subcategories of these popular inverters are symmetrical and asymmetrical inverters based on the features of the DC sources [13, 14]. Based on the control strategy of the power switches, MLIs can be classified into two main types: low frequency modulation and high frequency modulation [14-16]. The most common low frequency modulation techniques are selective harmonic elimination (SHE) and staircase wave synthesis. Low frequency modulation has low switching losses, and it is easy to implement [14, 16]. However, its dynamic behaviour is very poor where any changes in modulation index (MI) requires resolving what is called non-linear transcendental equations which is very difficult in real time operation. On the other hand, high frequency modulation provides more flexible control in real time operation and lower harmonic contents than low frequency modulation [17, 18]. Sinusoidal pulse width modulation (SPWM) is the most popular high frequency modulation. Multicarrier signals are usually employed in SPWM. Several multicarrier signals (based on the possible output voltage levels of the inverter) are compared with sinusoidal or rectified sinusoidal waveform. The intersections of the comparisons are the key of generating the required control signals of the power switches [19-23]. Very good performance is achieved when applying multicarrier based SPWM in MLIs with low level to high level MLIS. However, implementation of synchronized multicarrier signals has many problems especially with MLIs having many levels in the output voltage. The hardware is very complex and additional logic circuits are often required. This paper presents an effective approach that can overcome the problems associated with multicarrier

SPWM. The proposed approach, namely Higher Level Modulation does not employ any carrier signal. Instead of this, a rectified sine-wave is discretized into constant periods over the fundamental period. Each discrete value of this sine-wave lies between a higher level and a lower level. The proposed algorithm generates the control signals based on the range in which the sine-wave lies. Detailed analysis of the proposed approach is presented. The proposed approach in addition to conventional MCSPWM are applied to seven-level, thirteen-level, twenty-one level and thirty-one-level MLIs. Comparison between the proposed approach and MCSPWM is introduced. Simulation of the mentioned MLIs when applying the proposed approach is carried out to verify the effectiveness of the proposed approach. The paper is organized as follow: section 2 introduces the principal operation of the studied MLIs. Section 3 proposes principle of the proposed algorithm. Simulation and comparison between the proposed approaches and MCSPWM are presented in section 4. Section 5 presents Comparison between the proposed modulation technique and MCSPWM concludes the main points of the paper.

2. Principal operation of the presented MLIs

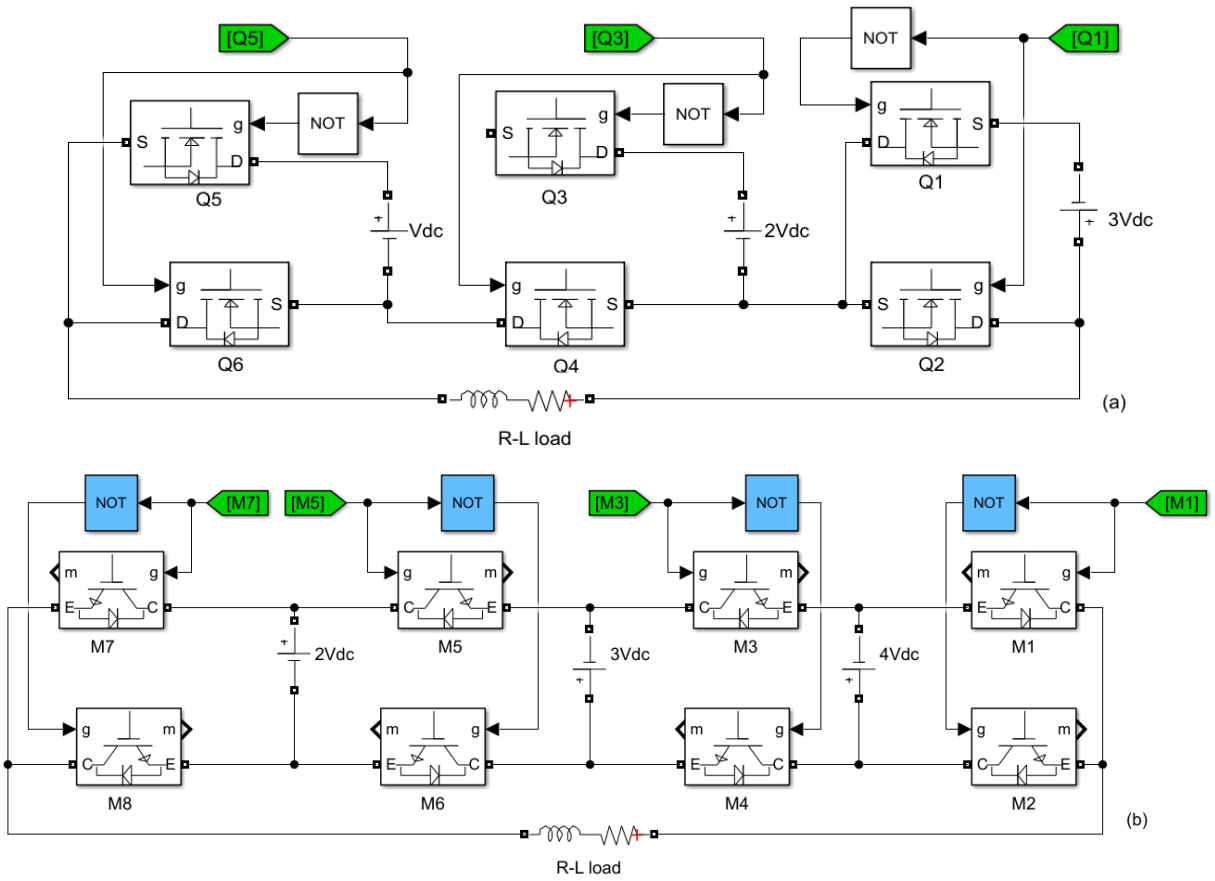
Multi-level inverter circuits are presented in figure 1 for (a) seven level MLI, (b) thirteen-level MLI, (c) twenty-one level MLI and (d) thirty-one-level MLI. For seven level MLI and 31-level MLI, each inverter consists of number of cells (m). 'm' equals 3 for seven level MLI and it equals 5 for 31-level MLI. The number of possible levels (N) for each inverter is:

$$N = 2^m - 1 \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Each cell includes a DC source and two switches in which they are turned on and off in a compliment mode. The voltage source in the far-left cell is set to V_{dc} and then the voltage source in each of the middle cells has a voltage of twice its left cell voltage. The voltage source in the far-right cell is set to V_R

$$V_R = \frac{N-1}{2} V_{dc} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The polarity of all sources is similar except the far-right cell. The connection of power switch terminals in all cells are similar except the far-right cell in which it is reversed. In case of 7-level inverter, the states of switches Q1, Q3 and Q5 are given in Table 1 with the corresponding load voltage V_0. The states of switches T1, T3, T5, T7 and T9 of the 31-level MLI are given in table 2 with the corresponding load voltage V_o. For 7-level and 31-level MLIs, the zero-output voltage is achieved by setting all odd numbered switches to the 'ON' state. The topology of the 13-level MLI shown in figure (1b) consists of eight power switches and three asymmetrical dc sources. The higher and lower switches in each mech are turned on and off in a compliment operation.



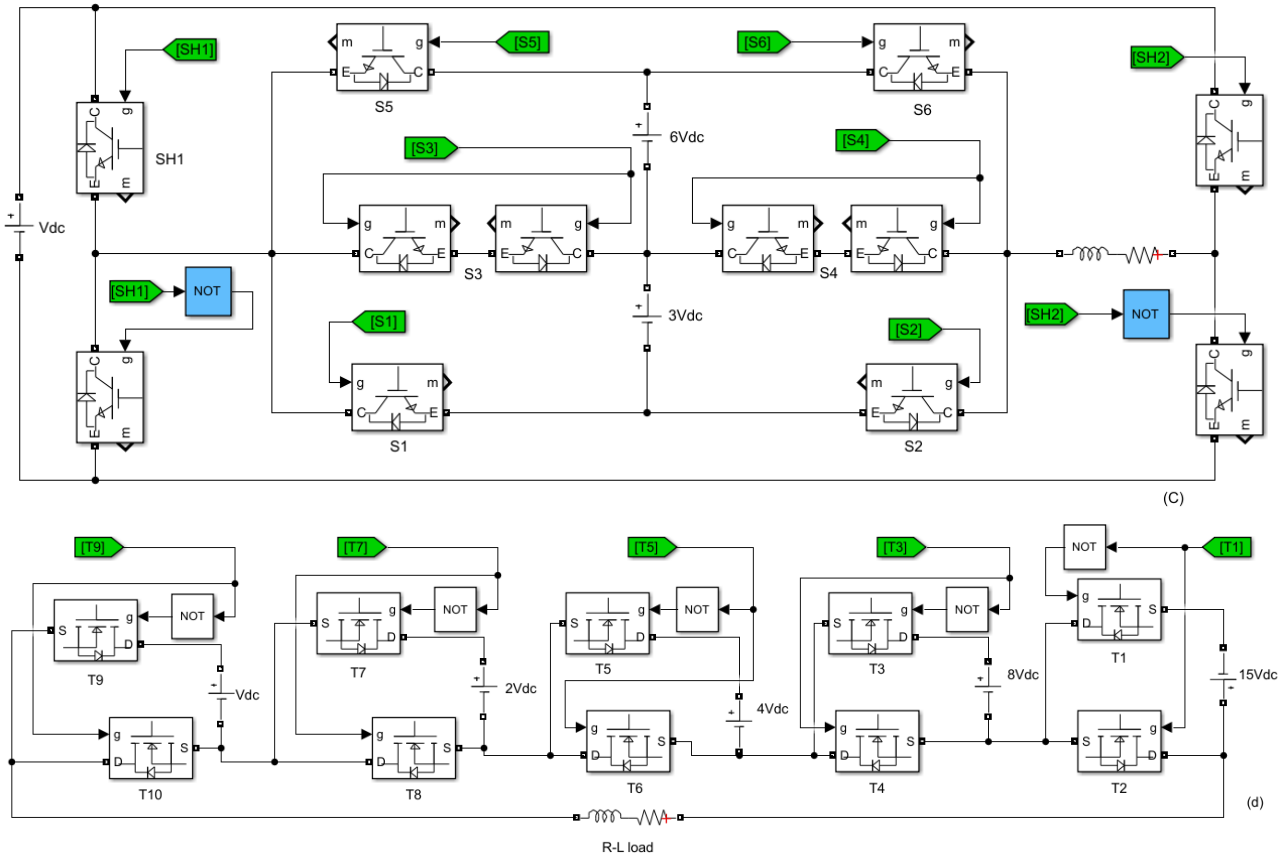


Figure 1: Multi level inverter circuits. (a) 7-level MLI, (b) 13-level MLI, (c) 21-level MLI and (d) 31-level MLI

The states of switches M1, M3, M5 and M9 of the 13-level MLI are given in table 3 with the corresponding load voltage V_o. For the three mentioned MLIs, the negative state for a certain output voltage is achieved by inverting all switches in the corresponding positive state. For instance, in 7-level inverter, the state 011 generates $3V_{dc}$while the state 100 generates $-3V_{dc}$. In 13-level inverter, the state 0100 generates $5V_{dc}$while the state 1011 generates $-5V_{dc}$. In 31-level inverter, the state 00110 generates $12V_{dc}$ while the state 11001 generates $-12V_{dc}$. Figure (1c) shows the 21-level MLI topology. The outer power switches operate at a high frequency switching and they are controlled by signals (SH1 and SH2) and their compliment signals. The inner power switches operate at a lower frequency. Three DC sources are utilized with values V_{dc}, $3V_{dc}$ and $6V_{dc}$. The states of power switches S1 through S6 in addition to SH1 and SH2 are given in table 4 with the corresponding load voltage V_o. In 21-level MLI, the compliment states of the power switches at a certain positive output voltage does not generate the corresponding negative output voltage as in 7-level, 13-level and 31-level MLIs.

Table 1: States of switches and corresponding inverter output voltage level (7-level MLI)

State No.	Q_5	Q_3	Q_1	V_o
1	1	1	0	$3V_{dc}$
2	0	1	0	$2V_{dc}$
3	1	0	0	V_{dc}
4	1	1	1	0
5	0	1	1	$-V_{dc}$
6	1	0	1	$-2V_{dc}$
7	0	0	1	$-3V_{dc}$

Table 2: States of switches and corresponding inverter output voltage level (31-level MLI)

State No.	T_9	T_7	T_5	T_3	T_1	V_0
1	1	1	1	1	0	$15V_{dc}$
2	0	1	1	1	0	$14V_{dc}$
3	1	0	1	1	0	$13V_{dc}$
4	0	0	1	1	0	$12V_{dc}$

State No.	T_9	T_7	T_5	T_3	T_1	V_0
5	1	1	0	1	0	$11V_{dc}$
6	0	1	0	1	0	$10V_{dc}$
7	1	0	0	1	0	$9V_{dc}$
8	0	0	0	1	0	$8V_{dc}$
9	1	1	1	0	0	$7V_{dc}$
10	0	1	1	0	0	$6V_{dc}$
11	1	0	1	0	0	$5V_{dc}$
12	0	0	1	0	0	$4V_{dc}$
13	1	1	0	0	0	$3V_{dc}$
14	0	1	0	0	0	$2V_{dc}$
15	1	0	0	0	0	V_{dc}
16	1	1	1	1	1	0

Table 3: States of switches and corresponding inverter output voltage level (13-level MLI)

State No.	M_7	M_5	M_3	M_1	V_o
1	0	1	1	0	$6V_d$
2	0	1	0	0	$5V_d$
3	1	1	1	0	$4V_d$
4	1	1	0	0	$3V_d$
5	0	1	1	1	$2V_d$
6	0	0	1	0	V_d
7	1	1	1	1	0
8	1	1	0	1	$-V_d$
9	1	0	0	0	$-2V_d$
10	0	0	1	1	$-3V_d$
11	0	0	0	1	$-4V_d$
12	1	0	1	1	$-5V_d$
13	1	0	0	1	$-6V_d$

Table 4: States of switches and corresponding inverter output voltage level (21-level MLI)

State No.	SH_2	SH_1	S_6	S_5	S_4	S_3	S_2	S_1	V_o
1	0	1	1	0	0	0	0	1	$10V_{dc}$
2	0	0	1	0	0	0	0	1	$9V_{dc}$
3	1	0	1	0	0	0	0	1	$8V_{dc}$
4	0	1	1	0	0	1	0	0	$7V_{dc}$
5	0	0	1	0	0	1	0	0	$6V_{dc}$
6	1	0	1	0	0	1	0	0	$5V_{dc}$
7	0	1	0	0	1	0	0	1	$4V_{dc}$
8	0	0	0	0	1	0	0	1	$3V_{dc}$
9	1	0	0	0	1	0	0	1	$2V_{dc}$
10	0	1	0	0	1	1	0	0	V_{dc}
11	0	0	0	0	1	1	0	0	0
12	1	0	0	0	1	1	0	0	$-V_{dc}$
13	0	1	0	0	0	1	1	0	$-2V_{dc}$
14	0	0	0	0	0	1	1	0	$-3V_{dc}$
15	1	0	0	0	0	1	1	0	$-4V_{dc}$
16	0	1	0	1	1	0	0	0	$-5V_{dc}$
17	0	0	0	1	1	0	0	0	$-6V_{dc}$
18	1	0	0	1	1	0	0	0	$-7V_{dc}$
19	0	1	0	1	0	0	1	0	$-8V_{dc}$
20	0	0	0	1	0	0	1	0	$-9V_{dc}$
21	1	0	0	1	0	0	1	0	$-10V_{dc}$

3. Principle of the proposed modulation technique

The principle of the proposed modulation can be explained with the help of Figure 2. The basic idea of conventional multicarrier based sinusoidal pulse width modulation MCSPWM is the individual comparison between the multi-carrier signals with a sinusoidal waveform (reference signal). Mathematical manipulation on the outputs of those comparisons in

addition to hardware logic circuits give the required control signals of the power switches. This conventional modulation suffers from the hardware complexity required for (1) generating the synchronized shifted multicarrier signals, (2) comparison between these signals and the reference sine-wave, (3) mathematical processing and logic circuits and (4) finally generating the required control signals. These problems increase as the number of inverter levels increases. Six shifted carrier signals are required for the 13-level MLI while 10 carrier signals and 15 carrier signals are required for the 21-level MLI and the 31-level MLI respectively. Another problem arises when very narrow pulse widths exist according to the changes in modulation index and consequently the change in discrete sine-wave values. The proposed modulation technique significantly reduces the mentioned problems associated with multicarrier sinusoidal pulse width modulation technique.

In the proposed modulation technique, the sine-wave reference signal is discretized in a number of samples per fundamental period equal to the number of carrier signal periods per fundamental period. During each carrier signal, the instantaneous discrete value of the sine-wave signal is determined. This value lies between two adjacent levels. The algorithm directly generates the control signals corresponding to the higher level of the adjacent levels. Referring to figure 2, an example of the sine-wave signal is a discrete value between the fourth and the fifth levels. For instance, and in case of 21-level MLI, without any comparison between carrier signals and sine-wave signal, the proposed algorithm generates the control signal 10100001 which results in an output voltage of $8V_{dc}$ if the sine-wave signals lies between the 7^{th} and 8^{th} carrier signals during positive half cycle. Another example in case of 31-level MLI, the algorithm generates the control signal 10110 which results in an output voltage of $13V_{dc}$ if the sine-wave signal lies between the 12^{th} and 13^{th} carrier signals during positive half cycle while the algorithm generates the control signal 01001 which results in an output voltage of $-13V_{dc}$ if the sine-wave signal lies between the 12^{th} and 13^{th} during negative half cycle. Each discrete value of the sine-wave signal is processed with the same manner when applying proposed modulation technique to the studied MLIs.

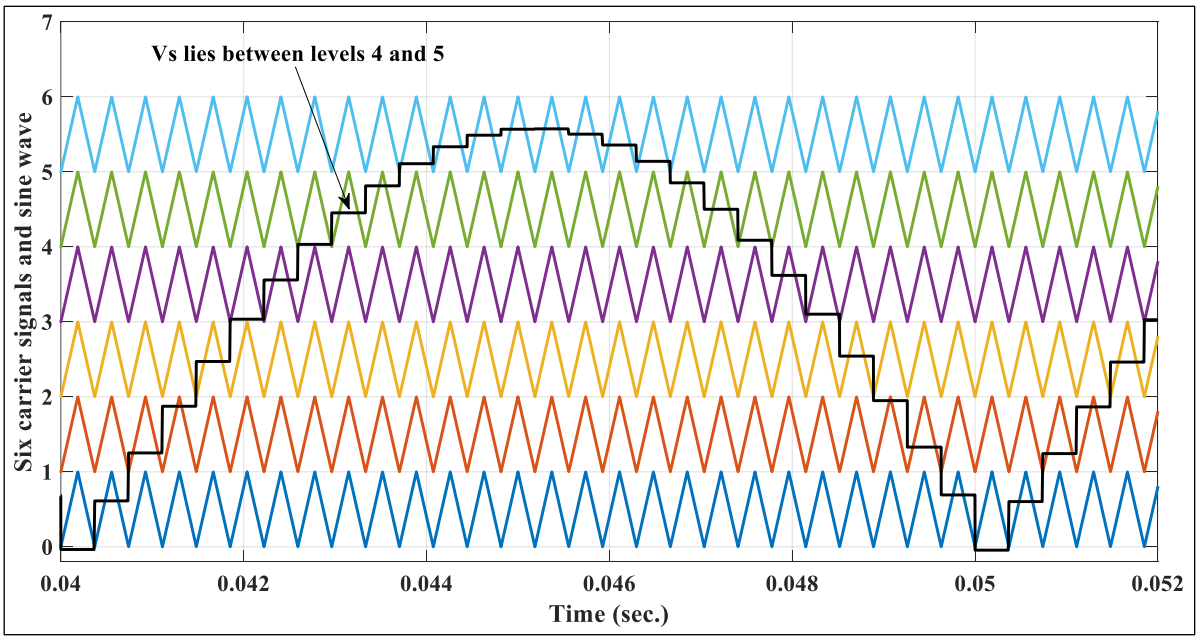


Figure 2: Principle of the proposed modulation method

4. Simulation results

The system is simulated using MATLAB/SIMULINK software for 7-level, 13-level, 21-level and 31-level multi level inverters. The fundamental frequency is set to 50 Hz. The frequency of the carrier signal is set to 2700 Hz to get 27 carrier cycles per half fundamental period. The maximum value of the sine-wave reference voltage is set to 300V which corresponds to modulation index=1. During simulation, the modulation index is set to 0.4 from 0s to 0.08s, then it is set to 0.6 from 0.08s to 0.16s, then it is set to 0.8 from 0.16s to 0.24s, then it is set to 1 from 0.24s to 0.32s. Therefore, four fundamental cycles are presented for each value of modulation index. The values of V_{dc} in each MLI are adjusted to get an output voltage of each inverter ranging from -300V to +300V. The load resistance is set to 10Ω while the load inductance is set to 20mH.

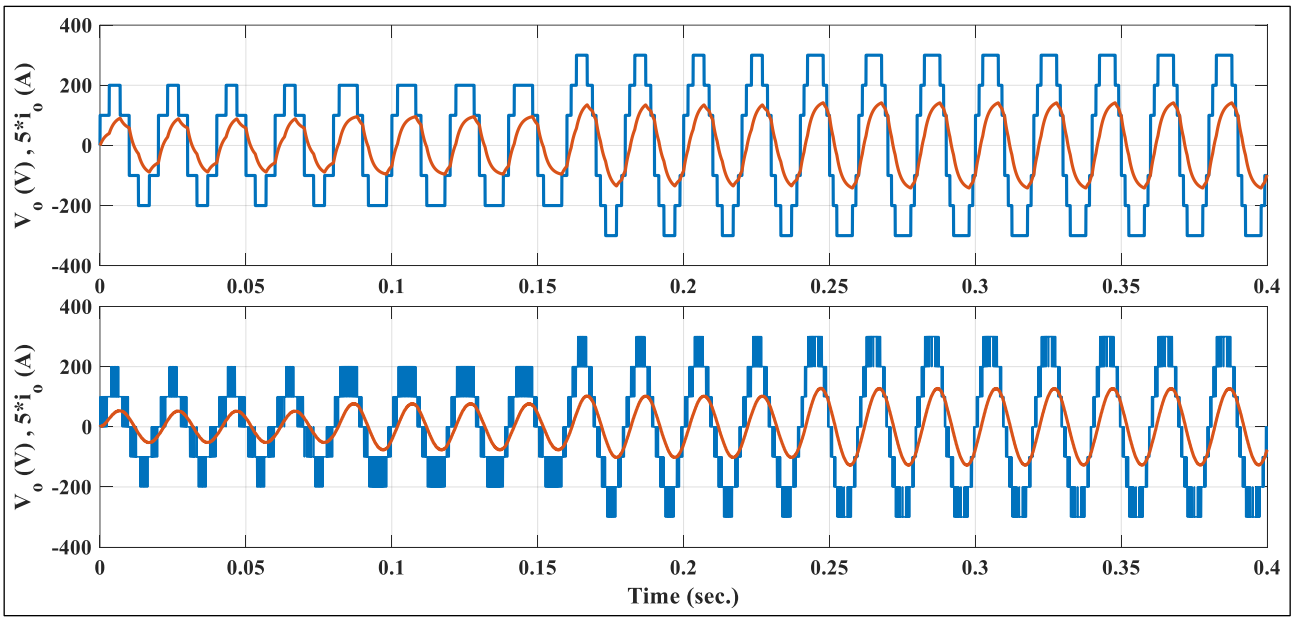
The proposed modulation technique is applied in addition to the conventional multicarrier sinusoidal pulse width modulation MCSPWM for the aim of performance comparison. First 7-level MLI is studied. Referring to figure 1a, the voltage sources are set to

100V, 200V and 300V. Figure 3a presents the inverter output voltage and current. With the proposed algorithm, the performance is poor compared to the results of MCSPWM especially at low modulation index. with MI greater than or equal 0.8, the performance becomes good considering the shape of load current. The second MLI is the 13-level. As in figure 1b, the voltage sources are set to 100V, 150V and 200V. Figure 3b presents the inverter output voltage and current. With the proposed algorithm, better performance is recognized compared to the results of 7-level inverter. With MI greater than or equal 0.6, the performance becomes very good considering the shape of load current. The third MLI is the 21-level. As in figure 1c, the voltage sources are set to 30V, 90V and 180V. Figure 3c presents the inverter output voltage and current. With the proposed algorithm, the performance is excellent when compared to the results of 7-level and 13-level inverters. With MI greater than or equal 0.4, the performance becomes excellent, and the load current is very close to sinusoidal shape. The last considered MLI is the 31-level. As in figure 1d, the voltage sources are set to 20V, 40V, 80V, 160V and 300V. Figure 3d presents the inverter output voltage and current. With the proposed algorithm, the performance is extremely excellent when compared to the results of 7-level and 13-level inverters. With MI greater than or equal 0.3, the performance becomes very excellent, and the load current is very close to sinusoidal shape.

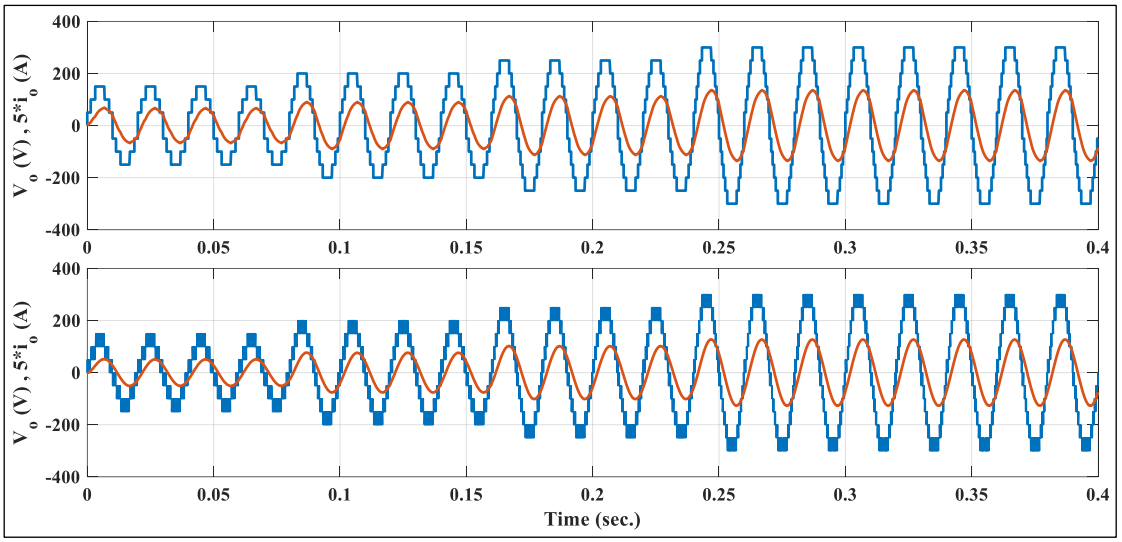
5. Comparison between the proposed modulation technique and MCSPWM

Detailed comparison between the proposed modulation technique and MCSPWM is presented. The comparison is carried out based on two criteria. The first is the total harmonic distortion of load current THD_{Io} while the root mean square of load voltage RMS_{Vo} is the second criteria. Tables 5 through 8 present the results of THD_{Io} and RMS_{Vo} when applying the proposed modulation technique in addition to the results when applying MCSPWM. As the THD_{Io} is a measure of harmonic contents in load current [24], it can be investigated that THD_{Io} is high in case of 7-level MLI except that if MI is 0.8 and 0.9 while THD_{Io} is improved with 13-level MLI where it becomes very small with MI $\geq$ 0.6. In case of 21-level MLI and 31-level MLI, THD_{Io} is extremely improved with MI $\geq$ 0.3.

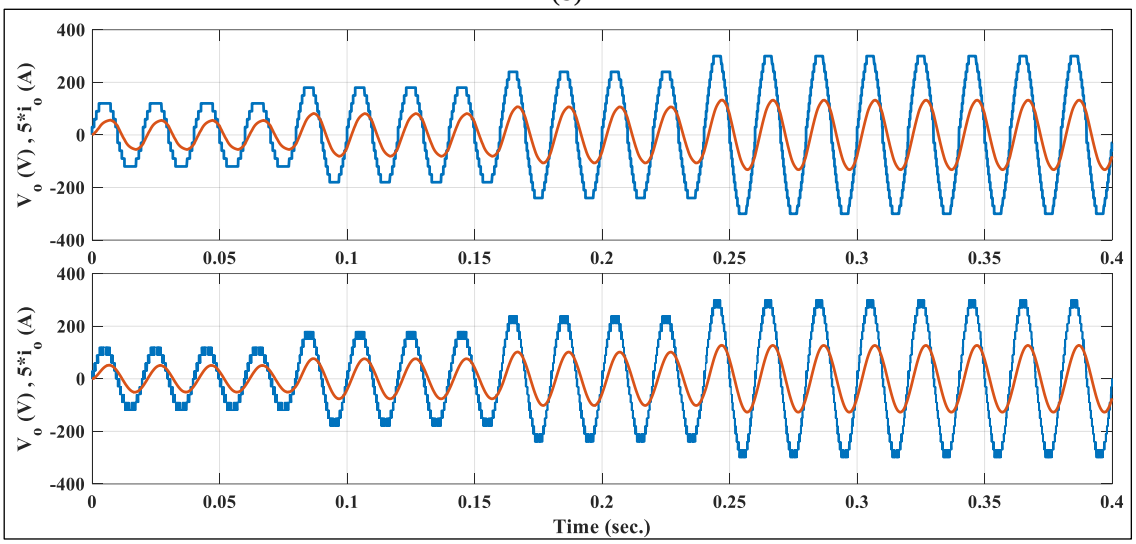
Considering RMS_{Vo}, it can be noticed that RMS_{Vo} with the proposed algorithm is always greater than that of MCSPWM as expected where the algorithm always generates the control signals corresponding to the upper level as previously explained in section 3. The deviation between RMS_{Vo} with the proposed modulation technique and RMS_{Vo} in case of MCSPWM is quite big in case of 7-level MLI. This deviation has the smallest values with 31-level MLI. In real time implementation, this problem can be easily addressed by readjusting the modulation index through controllers to achieve the required load voltage level.



(a)



(b)



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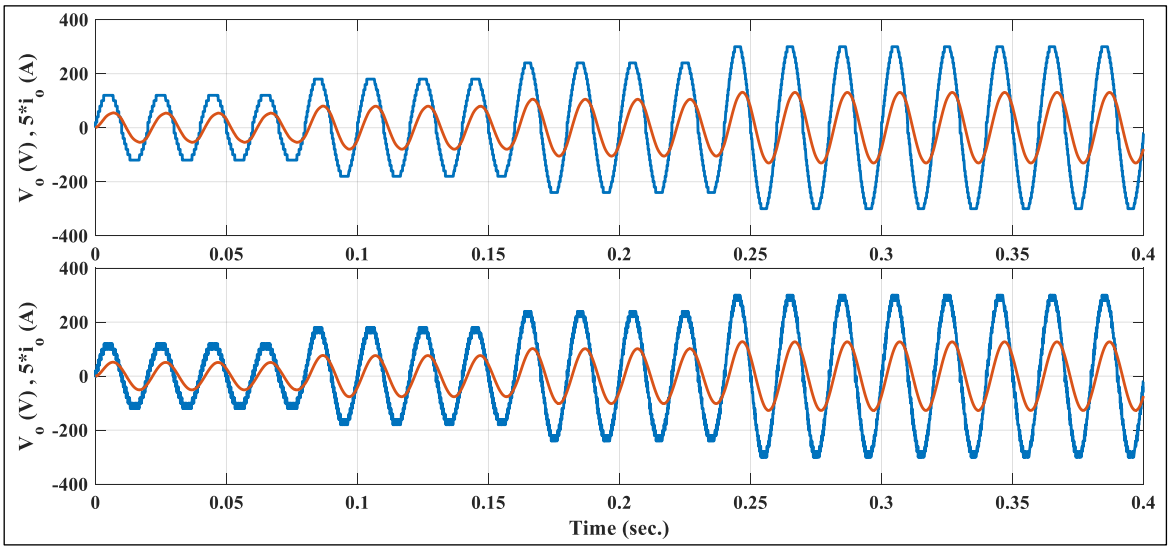

(d)

Figure 3: Load voltage (V) and load current (A) * 5 with step change in modulation index. (a) 7-level MLI (b) 13-level MLI (c) 21-level MLI and (d) 31-level MLI. In all figures, upper with the proposed algorithm while the lower is the MCSPWM

Table 5: Total harmonic distortion of load current and root mean square of load voltage (7-level MLI)

MI	Proposed modulation technique		Conventional MCSPWM	
	THD of I_o (%)	RMS of V_0 (V)	THD of I_o (%)	RMS of V_0 (V)
0.1	20.4	100	6.2	43.6
0.2	20.4	100	2.97	61.6
0.3	20.4	100	2.5	76.8
0.4	7.6	145.7	1.7	93.3
0.5	6.4	161.4	1.9	113.6
0.6	8.8	169.5	1.3	133.5
0.7	5.6	201	0.98	152.8
0.8	3.9	224.7	0.97	175
0.9	4.9	236.6	1.2	195.9
1	6.8	245.5	0.7	215.5

Table 6: Total harmonic distortion of load current and root mean square of load voltage (13-level MLI)

MI	Proposed modulation technique		Conventional MCSPWM	
	THD of I_o (%)	RMS of V_0 (V)	THD of I_o (%)	RMS of V_0 (V)
0.1	20.4	50	2	30.8
0.2	7.6	72.76	0.75	46.4
0.3	8.6	84.7	0.64	67
0.4	3.6	112.3	0.47	87.2
0.5	6.8	122.7	0.39	107.7
0.6	3.3	151.6	0.37	129
0.7	2.45	174.5	0.33	149.7
0.8	3.1	191	0.33	171
0.9	1.9	216.4	0.3	192.1
1	3.1	230.1	0.29	213.1

Table 7: Total harmonic distortion of load current and root mean square of load voltage (21-level MLI)

MI	Proposed modulation technique		Conventional MCSPWM	
	THD of I_o (%)	RMS of V_0 (V)	THD of I_o (%)	RMS of V_0 (V)
0.1	20.4	30	0.9	23.9
0.2	10.2	52	0.5	43.95
0.3	6.7	73.7	0.36	64.7
0.4	4.9	95.2	0.28	85.6
0.5	3.9	116.7	0.22	106.7
0.6	3.2	138.1	0.21	127.9
0.7	2.9	159.5	0.2	149
0.8	2.3	180.8	0.18	170.1
0.9	2	202.1	0.17	191.3
1	1.8	223.4	0.15	212.4

Table 8: Total harmonic distortion of load current and root mean square of load voltage (31-level MLI)

MI	Proposed modulation technique		Conventional MCSPWM	
	THD of I_o (%)	RMS of V_0 (V)	THD of I_o (%)	RMS of V_0 (V)
0.1	6.1	32.3	0.71	22.9
0.2	6.7	49.1	0.32	43.1
0.3	2.3	73.7	0.26	64.2
0.4	3.2	92	0.2	85.2
0.5	1.44	115.8	0.18	106.4
0.6	2	134.7	0.17	127.5
0.7	1.1	158.1	0.17	148.7
0.8	1.5	177.3	0.17	169.9
0.9	0.84	200.4	0.19	191
1	1.1	219.9	0.17	212

5. CONCLUSION

An effective modulation technique is proposed for MLIs operation. The proposed modulation technique overcomes the problems associated with multicarrier SPWM. The reference rectified sinusoidal waveform is discretized to 54 periods over the fundamental period. Each discrete value of the reference signal lies between two levels of the inverter possible levels. Once the range in which the reference signal lies, the proposed approach can be applied. The control signals are generated to get the higher-level voltage. The proposed approaches in addition to MCSPWM are applied to 7-level, 13-level, 21-level and 31-level MLIs and the systems for all cases are simulated then compared using MATLAB/SIMULINK. Simulation results show that the proposed approach provides very good performance with 13-level MLI operating at MI $\geq$ 0.6 and excellent performance in case of 21-level and 31-level MLIs operating at MI $\geq$ 0.3. Poor performance is recognized in case of 7-level MLI. Fortunately, with low levels MLIs like 7-level MLI, implementation of MCSPWM is not so difficult and therefore there is no need to apply the proposed algorithm. On the other hand, with high levels MLIs like 21-level and 31-level MLIs, implementation of MCSPWM becomes very difficult and thus the proposed algorithm will be very effective to apply. The proposed approach combines the simplicity of low frequency modulation and the high performance of high frequency modulation in MLIs having many output voltage levels.

REFERENCES

1. Mali, R., Adam, N., Satpaise, A., & Vaidya, A. P. (2019, February). Performance comparison of two level inverter with classical multilevel inverter topologies. In *2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)* (pp. 1-7). IEEE.
2. Kumar, B. H., & Lokhande, M. M. (2017, October). Analysis of PWM techniques on multilevel cascaded H-Bridge three phase inverter. In *2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE)* (pp. 465-470). IEEE.
3. Ahmed, M., & Hendawi, E. (2016). A new single-phase asymmetrical cascaded multilevel DC-link inverter. *Journal of Power Electronics*, *16*(4), 1504-1512.
4. Hussein, T. A. (2021). Multilevel level single phase inverter implementation for reduced harmonic contents. *International Journal of Power Electronics and Drive Systems*, *12*(1), 314-324.
5. Kakar, S., Ayob, S. M., Arif, M. S., Nordin, N. M., Daud, Z., & Ayop, R. (2021). A new multilevel inverter topology based on switched-capacitor. *International Journal of Power Electronics and Drive Systems (IJPEDS)*, *12*(1), 627-636.
6. Shobini, M. M., Kamala, J., & Rathna, R. (2017, February). Analysis and simulation of flying capacitor multilevel inverter using PDPWM strategy. In *2017 International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)* (pp. 91-95). IEEE.
7. Porselvi, T., & Muthu, R. (2011, December). Comparison of cascaded H-Bridge, neutral point clamped and flying capacitor multilevel inverters using multicarrier PWM. In *2011 Annual IEEE india conference* (pp. 1-4). IEEE.
8. Kakar, S., Ayob, S. M., Arif, M. S., Nordin, N. M., Daud, Z., & Ayop, R. (2021). A new multilevel inverter topology based on switched-capacitor. *International Journal of Power Electronics and Drive Systems (IJPEDS)*, *12*(1), 627-636.
9. Chlaihawi, A., Sabbar, A., & Jedi, H. (2020). A high-performance multilevel inverter with reduced power electronic devices. *International Journal of Power Electronics and Drive Systems*, *11*(4), 1883-1889.
10. Dong, X., Yu, X., Yuan, Z., Xia, Y., & Li, Y. (2016). An improved SPWM strategy to reduce switching in cascaded multilevel inverters. *Journal of Power Electronics*, *16*(2), 490-497.
11. Prakash, G., Balamurugan, M., & Umashankar, S. (2014). A new multilevel inverter with reduced number of switches. *International Journal of Power Electronics and Drive Systems*, *5*(1), 63.
12. Haq, S., Biswas, S. P., Hosain, M. K., Rahman, M. A., Islam, M. R., & Jahan, S. (2021). A modular multilevel converter with an advanced PWM control technique for grid-tied photovoltaic system. *Energies*, *14*(2), 331.
13. Kumar, K. V., & Kumar, R. S. (2019). Analysis of logic gates for generation of switching sequence in symmetric and asymmetric reduced switch multilevel inverter. *IEEE Access*, *7*, 97719-97731.
14. Ahmed, M., Hendawi, E., & Metwaly, M. K. (2018). Single Phase Asymmetrical Cascaded MLI with Extreme Output Voltage Levels to Switch Ratio. *International Journal of Power Electronics and Drive Systems (IJPEDS)*, *9*(2), 712-721.
15. Prabaharan, N., & Palanisamy, K. (2017). A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications. *Renewable and Sustainable Energy Reviews*, *76*, 1248-1282.
16. Ahmed, M., Hendawi, E., Alamri, B., Alharthi, M., Salem, F., Orabi, M., ... & Ghoneim, S. (2020). Classical Control for Unequal DC Sources Five-Level Inverter-Based SHE Technique. *Energies*, *13*(18), 4715.
17. Sahoo, S. K., & Bhattacharya, T. (2017). Phase-shifted carrier-based synchronized sinusoidal PWM techniques for a cascaded H-bridge multilevel inverter. *IEEE Transactions on Power Electronics*, *33*(1), 513-524.

18. Kumar, K. V., & Kumar, R. S. (2018). Advanced PWM techniques for control of power electronic converters in PV and motor drive systems. *Int. J. Pure Appl. Math.*, *118*(24), 1-21.
19. Ye, M., Chen, L., Kang, L., Li, S., Zhang, J., & Wu, H. (2019). Hybrid multi-carrier PWM technique based on carrier reconstruction for cascaded H-bridge inverter. *IEEE Access*, *7*, 53152-53162.
20. Tan, L., Wu, B., Narimani, M., Xu, D., & Joós, G. (2017). Multicarrier-based PWM strategies with complete voltage balance control for NNPC inverters. *IEEE Transactions on Industrial Electronics*, *65*(4), 2863-2872.
21. Mahato, B., Majumdar, S., & Jana, K. C. (2018). Carrier-based PWM techniques for multi-level inverters: a comprehensive performance study. *Gazi University Journal of Science Part A: Engineering and Innovation*, *5*(3), 101-111.
22. Gopalakrishnan, K., Raj, M. S., & Saravanan, T. (2014). Harmonic evaluation of multicarrier PWM techniques for cascaded multilevel inverter, *Middle-East J Sci Res*, *20*(7), 819–824.
23. Kumar, K. V., & Kumar, R. S. (2019). Analysis of logic gates for generation of switching sequence in symmetric and asymmetric reduced switch multilevel inverter. *IEEE Access*, *7*, 97719-97731.
24. IEEE Recommended Practices & Requirements for Harmonic Control in Electrical Power Systems, IEEE Standard 519-2014.